REMARKS/ARGUMENTS

The Examiner is thanked for the Office Action dated April 20, 2007.

The status of the application is as follows:

- Claims 21-40 are pending and are presently under consideration. Claim 21 has been amended to include aspects of cancelled claim 23.
- Claims 21-40 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of co-pending Application No. 10/730,319.
- Claims 21-27, 29, 31, 32, 34-36, 38, and 40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann, *et al.* (U.S. Publication No. 2002/0169922) in view of Pollard, *et al.* (US 7,050,959).
- Claims 28, 33, and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann, *et al.* in view of Pollard, *et al.* and further in view of Mylly (US Publication No. 2005/0235110).
- Claims 30 and 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann, *et al.* in view of Pollard, *et al.* and further in view of Jeddeloh (US Publication No. 2002/0144173).
- These rejections are discussed below.

The Provisional Rejection of Claims 21-40 on the Ground of Nonstatutory Obviousness-Type Double Patenting

Claims 21-40 stand provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-15 of co-pending Application No. 10/730,319. This rejection will be addressed in the event that Application No. 10/730,319 issues as a patent.

The Rejection of Claims 21-27, 29, 31, 32, 34-36, 38, and 40 Under 35 U.S.C. §103(a)

Claims 21-27, 29, 31, 32, 34-36, 38, and 40 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann, *et al.* in view of Pollard, *et al.* Withdrawal of this rejection is respectfully requested, as the cited references, alone or in combination, fail to teach or suggest each and every aspect as recited in these claims.

> To establish a *prima facie* case of obviousness... the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP §2142

Claims 21, 34, and 40

Claim 21 has been amended to include aspects of cancelled claim 23, and recites, *inter alia, receiving memory attachment position information that indicates memory slots to which each of the multiple memory modules is attached, individually determining data transfer rates for each memory module in the multiple memory modules based at least in part upon the corresponding received memory module attribute information and the attachment position information, and collectively setting a data transfer rate with respect to the multiple memory modules based at least in part on the individually determined data transfer rates.* Claims 34 and 40 recite similar aspects.

Thomann, *et al.* is directed to determining a data clock delay time in memory devices. In more detail, as disclosed in Thomann, *et al.,* a particular delay must exist with respect to a "read" operation between when a first latch (150) receives a signal (DATA CLK) indicating that data in a memory cell should be latched to an output buffer (148) and when a second latch (25) in a memory controller receives a signal (R/W CLK) to receive data from a DQ pad (140) that received the data from the output buffer (148). Similarly, a particular delay must exist with respect to a "write" operation between when the second latch (25) receives a signal (R/W CLK) to latch data to the DQ pad (140) (and thus to an input buffer 144) and when the first latch (150) receives a signal (DATA CLK) indicating that data in the input buffer 144 is to be latched to a memory cell. If the amount of delay between the DATA CLK signal and the R/W signal (or *vice versa*) is incorrect, incorrect data may be read from the input buffer or the output buffer.[1]

As cited by the Examiner, Thomann, *et al.* additionally teaches that a data clock delay can be determined at an input/output line (DQ line) level, at a memory device level, at a memory module level, or at a system level. Specifically, Thomann, *et al.* discloses that, for memory device level calibration, a single data clock delay is selected to provide reliable transfer on all DQ lines of a memory device (e.g., a single data clock delay is used on all DQ lines of the memory device). For memory module level calibration, a single data clock delay is selected to provide reliable transfer on all DQ lines of the memory module. For system level calibration, a single data clock delay is selected to provide reliable transfer on all DQ lines of a computer system, such that data

[1] Thomann, *et al.,* paragraphs [0039] – [0045]

transmission on any DQ line in the computer system is performed using the single data clock delay.[2]

The Examiner concedes that Thomann, *et al.* does not receive memory module attachment position information, much less determining a data transfer rate based upon the attachment position information, and cites Pollard, *et al.* to teach such claimed aspects. Pollard, *et al.* discloses determining a sustainable power level of a memory module, translating that power level into a performance characteristic, and using the memory module such that the performance characteristic is not exceeded.[3] Pollard, *et al.*, however, is silent with respect to using attachment position information to determine a sustainable power level of a memory module. The portion cited by the Examiner states that module design characteristics can include a number of devices on a module, active, idle, and standby power consumption levels of each device on the module, substrate height, heat spreader design data, and a maximum allowable junction temperature.[4] Pollard, *et al.* nowhere discloses that attachment position information for a memory module is received. In addition, the formulas disclosed in Pollard, *et al.* use junction temperature of a memory module, ambient temperature of a system chassis, a power level for active idle devices, a power level for devices in standby mode, and a power level for devices in nap mode.[5] Thus, Pollard, *et al.* is entirely silent with respect to using attachment position information of a memory module to compute a data transfer rate for the memory module as required by this claim.

Accordingly, as the combination of Thomann, *et al.*, and Pollard, *et al.* fail to teach or suggest each and every aspect as recited in this claim, withdrawal of this rejection is respectfully requested.

Claims 25 and 35

Claim 25 recites *accessing a setting value candidate database, and retrieving a data transfer rate from the setting value candidate database for at least one memory module in the multiple memory modules, the data transfer rate from the setting value candidate database is located based at least in part upon memory attribute information stored in the at least one memory module*. Claim 35 recites similar aspects. The portions of Pollard, *et al.* cited by the Examiner as teaching these claimed aspects relate to influence coefficients (A, B, C, D) used in an equation to

[2] Thomann, *et al.*, paragraph [0063]
[3] Pollard, *et al.*, Fig. 2
[4] Pollard, *et al.*, col. 3, lines 30-40
[5] Pollard, *et al.*, col. 4, lines 5-14

determine a maximum sustainable power level for an integrated circuit, which is in turn used to determine an average allowable bandwidth for the integrated circuit.[6] Pollard, *et al.* additionally discloses that these influence coefficients may be stored in a BIOS along with influence coefficients for several other system platforms, and that the BIOS may use a lookup table to determine the appropriate influence coefficients. It is readily apparent, then, that these influence coefficients are not data transfer rates as required by this claim. In addition, the influence coefficients are discloses as being environmental characteristics of a computer system (airflow rates, module layout, motherboard layout). Therefore, it is not clear how these are located *based at least in part upon memory attribute information stored in the at least one memory module* as claimed. Therefore, this rejection should be withdrawn.

Claim 27

Claim 27 recites, *inter alia, determining a maximum data transfer rate with respect to data transfer rates determined for each memory module, determining a minimum data transfer rate with respect to data transfer rates determined for each memory module, and collectively setting the data transfer rate with respect to the multiple memory modules as a value that is between the maximum data transfer rate and the minimum data transfer rate.* Pollard, *et al.* does not disclose determining transfer rates for multiple memory modules, and thus cannot determine a minimum transfer rate and a maximum transfer rate for a plurality of memory modules, respectively. In addition, the portion cited in the Office Action for collectively setting transfer rates for multiple memory modules refers only to a single memory module. Accordingly, the rejection of this claim should be withdrawn.

Claim 31

Claim 31 recites, *inter alia, determining a first data transfer rate setting value for the first memory module based at least in part upon the acquired first memory attribute information, determining a second data transfer rate setting value for the second memory module based at least in part upon the acquired second memory attribute information, and determining a data transfer rate setting value that is to be applied to the first memory module and the second memory module based at least in part upon the analysis of the first data transfer setting value and the second data transfer rate setting value.* In contrast to the assertions in the Office Action, Thomann, *et al.* does

[6] Pollard, *et al.*, col. 4, 15-17

not teach or suggest these claimed aspects.

As noted above, Thomann, *et al.* teaches determining data clock delay times in memory devices. These times can be assigned at the input/output line (DQ line) level, at the memory device level, at the memory module level, or at the system level. However, determining a data clock delay time at the system level does not involve individually determining data clock delay times for each module in the system. Instead, the system-level data clock delay time is selected such that reliable data transfer is provided on all DQ lines of a computer system. There is no teaching or suggestion in Thomann, *et al.* of calculating data clock delay times for two or more modules and using such calculated data clock delay times to determine a system data clock delay time. Pollard, *et al.* likewise does not teach or suggest the above claimed aspects, and accordingly the rejection of this claim should be withdrawn.

Claim 36

Claim 36, which depends from claim 31, recites, *inter alia, determining the first data transfer rate setting value based at least in part upon the first upper limit temperature, determining the second data transfer rate setting value based at least in part upon the second upper limit temperature, analyzing the first data transfer rate setting value and the second data transfer rate setting value, and determining a data transfer rate setting value that is to be applied to the first memory module and the second memory module based at least in part upon the analysis of the first data transfer setting value and the second data transfer rate setting value.*

The portions of Pollard, *et al.* cited by the Examiner discloses receiving a maximum junction temperature and using such temperature to compute a maximum sustainable power level for a memory module.[7] However, neither Pollard, *et al.* or Thomann, *et al.* teach or suggest determining a data transfer rate setting that is collectively applied to two memory modules based upon individually determined data transfer rate settings for each of the two memory modules, wherein the individually determined data transfer settings are based upon upper limit temperatures of each of the two memory modules. Accordingly, withdrawal of this rejection is respectfully requested.

[7] Pollard, *et al.*, col. 3, lines 30-48

Claim 38

Independent claim 38 recites, *inter alia, accessing a setting value candidate database; locating candidate data transfer rate setting values for each memory module in the plurality of memory modules in the setting value candidate database, wherein the candidate data transfer rate setting values correspond to the acquired memory attribute information in the setting value candidate database; and determining a data transfer rate setting value that is to be applied with respect to each memory module in the plurality of memory modules based at least in part upon the located candidate data transfer rate setting values.*

As noted above, and in contrast to assertions in the Office Action, Pollard, *et al.* fails to disclose locating data transfer rate setting values in a lookup table for memory modules, and instead teaches accessing lookup coefficients in a BIOS, wherein the lookup coefficients are parameters used to determine a maximum sustainable power level for a given integrated circuit. Accordingly, neither Pollard, *et al.* or Thomann, *et al.* can teach determining a data transfer rate setting value that is to be applied to multiple memory modules based at least in part upon located candidate data transfer rate setting values as required by this claim. Therefore, withdrawal of the rejection of this claim is respectfully requested.

Claims 22, 24, 26, 29, and 32

These claims are believed to be allowable at least by virtue of their dependencies from their respective base claims.

The Rejection of Claims 28, 33, and 39 Under 35 U.S.C. §103(a)

Claims 28, 33, and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann, *et al.* in view of Pollard, *et al.* and further in view of Mylly. This rejection should be withdrawn, as these claims are believed to be allowable at least by virtue of their dependencies from their respective base claims.

The Rejection of Claims 30 and 37 Under 35 U.S.C. §103(a)

Claims 30 and 37 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Thomann, *et al.* in view of Pollard, *et al.* and further in view of Jeddeloh. Withdrawal of this

rejection is respectfully requested, as claims 30 and 37 are believed to be in condition for allowance at least by virtue of their dependencies from their respective base claims.

Conclusion

It is believed that each of the claims now in the application is distinguishable one from the other and over the prior art. Therefore, reconsideration and allowance of the claims is respectfully requested.

Respectfully submitted,

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